



Docket No.: 50432-477

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

William G. EN, et al.

Serial No.: 10/021,497

Group Art Unit: 2822

Filed: December 19, 2001

Examiner: SOWARD, Ida M.

For: ARRAY OF GATE DIELECTRIC STRUCTURES TO MEASURE GATE  
DIELECTRIC THICKNESS AND PARASITIC CAPACITANCE

10/A Amdt  
2-25-03  
A. Walker

AMENDMENT

Commissioner for Patents  
Washington, DC 20231

Sir:

The following amendments and remarks are respectfully submitted in response to  
the Office Action dated November 20, 2002.

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IN THE SPECIFICATION:

Please replace the paragraph beginning at page 7, line 9, with the following  
rewritten paragraph:

--In other embodiments different gate dielectric layers are formed on a wafer  
comprising shallow trench isolation regions. FIG. 8 illustrates a wafer 150 comprising a  
silicon base layer 152 and a plurality of shallow trench isolation regions 154. A gate  
oxide layer 156 is formed on the silicon base layer 152 by thermal oxidation of silicon  
layer 152 or by silicon oxide deposition techniques. After the formation of the gate oxide  
layer 156, a mask is formed over the wafer 150 and selected first portions of the gate  
oxide layer 156 are removed by etching. A first alternate dielectric is subsequently